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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,774	01/12/2004	Edward Herbert		1773

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,774	HERBERT, EDWARD	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12 and 13* is/are rejected.

7)☒ Claim(s) *9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1 and 8-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-11 and 14-17 of copending Application No. 10248438. Although the conflicting claims are not identical, they are not patentably distinct from each other because they both recite the same scope.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

Claim 1 is objected because the phase "a first MOSFET comprising a first MOSFET" in line 3 is confusing. Correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 7, 8 and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by Parks (USP 6208535).

As to claims 1 and 12, Parks discloses in figure 6A a MOSFET and a gate drive circuit adapted for very fast turn off for reduced crossover power losses, and a method thereof, comprising a first MOSFET comprising a first MOSFET (IRFP250) having a gate, a drain and a source for switching a load current (current going through 606) equal to i_d ; at least a second MOSFET (TN07) having a gate, a drain and a source for turning off the first MOSFET; the source of the first MOSFET and the source of the at least a second MOSFET being connected together as a source connection, the gate of the first MOSFET and the drain of the at least a second MOSFET being connected together as a drain-gate connection, the gate of the first MOSFET being characterized by having a very low gate resistance (when transistor TN07 is on, its resistance is low. Thus, the gate resistance of transistor IRFP250 is low when transistor TN07 is on), the on resistance of the at least a second MOSFET being characterized by having a very low channel resistance (when the transistor is fully on), the source connection being characterized by having a very low impedance, and the drain-gate connection being characterized by having a very low impedance, so that when the at least a second MOSFET is turned on, a gate current i_g will flow from the gate of the first MOSFET to the source of the first MOSFET through the at least a second MOSFET (because the resistance of transistor TN07 is low when on, all currents will be grounded through transistor TN07), and the gate current i_g is

larger than the Iload current i_d. (when transistor TN07 is on, transistor IRFP250 is off. The load current is 0).

As to claim 2, figure 6A shows the at least a second MOSFET is a large number of second MOSFETS (figure 6A shows two TN07 transistors); the source connection is a large number of source connections, and the drain-gate connection is a large number of drain-gate connections.

As to claim 3, figure 6A shows the large number of second MOSFETS are integrated into the first MOSFET die.

As to claim 8, figure 6A shows a gate turn on circuit comprising at least a third MOSFET (LP07) connected to a source of voltage (6V) and an inductor (connected to drain of LP07) connected to the at least a third MOSFET and to the gate of the first MOSFET.

5. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinzer et al. (USP 6593662).

As to claim 1, Kinzer et al. discloses in figure 7 a MOSFET (1) and a gate drive circuit (2, 3) adapted for very fast turn off for reduced crossover power losses (the "adapted for very fast turn off for reduced crossover power losses" limitation is merely a statement of intended use and as such, not given patentable weight), comprising a first MOSFET (1) comprising a first MOSFET die having a gate (G1), a drain 9D1) and a source (S1) for switching a load current equal to i_d; at least a second MOSFET (3) comprising at least a second MOSFET die having a gate (G3), a drain (D3) and a source (S3) for turning off the first MOSFET; the source of the first MOSFET and the source of the at least a second MOSFET being connected together as a source connection; the gate of the first MOSFET and the drain of the at least a second MOSFET being

connected together as a drain-gate connection; the gate of the first MOSFET being characterized by having a very low gate resistance (when transistor 3 is on, it's resistance is low. Thus, the resistance at the gate G1 is low); the on resistance of the at least a second MOSFET being characterized by having a very low channel resistance (when transistor 3 is on, it's resistance is low); the source connection being characterized by having a very low impedance (because the sources are connected directly, the resistance between the sources is low); and the drain-gate connection being characterized by having a very low impedance (the drain G3 is directly connected to the gate G1, therefore, the resistance between the drain D3 and the gate G1 is low), so that when the at least a second MOSFET is turned on, a gate current i_g will flow from the gate of the first MOSFET to the source of the first MOSFET through the at least a second MOSFET, and the gate current i_g is larger than the load current i_d (transistor 1 is off when transistor 3 is on. Thus, there is no current going through transistor 1. Therefore, the current going through transistor 3 is greater than the current going through transistor 1).

As to claim 12, figure 7 shows a method comprising fabricating the first MOSFET (1) so as to have a very low gate resistance, fabricating at least a second MOSFET (3) comprising at least a second MOSFET die and having a drain (D3), a gate (G3) and a source (S3) so that the on resistance of the at least a second MOSFET is very low; connecting the source (S1) of the first MOSFET to the source of the at least a second MOSFET with a source connection having a very low impedance; connecting the gate (G1) of the first MOSFET to the drain of the at least a second MOSFET with a gate-drain connection having a very low impedance; and turning on the at least a second MOSFET so that a current i_g will flow from the gate of the first MOSFET to the

source of the first MOSFET through the at least a second MOSFET, and the gate current i_g is larger than the load current i_d.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer et al. (USP 6593622) in view of Parks (USP 6208535).

As to claims 2 and 3, Kinzer et al.'s figure 7 shows a MOSFET and a gate driver circuit comprising a first MOSFET (2) a second MOSFET (3) having source connected to the source of the first MOSFET and having drain connected to the gate of the first MOSFET. Thus, figure 7 shows all limitations of the claim except for plurality of second MOSFETs connected in parallel. However, Parks' figure 6A shows a second MOSFET circuit (TN07s) having plurality of second MOSFETs connected in parallel for reducing the total impedance of the second MOSFET circuit, thereby turning off the first MOSFET faster. Therefore, it would have been obvious to one having ordinary skill in the art to modified Kinzer et al.'s second MOSFET with a plurality of second MOSFETs connected in parallel for the purpose of improving circuit speed.

As to claim 4, the modified Kinzer et al.'s figure 3 shows that the first MOSFET comprises a first MOSFET die (1) and the large number of second MOSFETS comprise a second MOSFET die (3), and the at least a second MOSFET die is immediately proximate to the first MOSFET die.

As to claim 5, the modified Kinzer et al.'s figures 8 and 9 shows that the second MOSFET die is mounted upon the first MOSFET die.

As to claim 6, the modified Kinzer's figures 7 and 6 shows that the plurality of second MOSFETs are mounted upon the first MOSFET die and connected thereto as a hybrid circuit.

8. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Preslar et al. (USP 5347169) in view of Parks (USP 6208535).

Preslar et al.'s figure 1 shows a MOSFET and a gate driver circuit comprising a first MOSFET (N1) a second MOSFET (NA in figure 2) having source connected to the source of the first MOSFET and having drain connected to the gate of the first MOSFET; a local clamp circuit D1 comprising diode immediate proximate to the first MOSFET. Thus, figure 7 shows all limitations of the claim except the local clamp circuit further comprises a capacitor. However, Parks 's figure 6A shows capacitor (such as the 1μF coupled to 50Vdc) coupled to the supply voltage for stabilizing the supply voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor coupled between Vcc and ground for the purpose of stabilizing Vcc).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (USP 6127861) in view of Wanlass (USP 3356858).

Lee's figure 2 shows an apparatus comprising a first MOSFET (N14) comprising a first MOSFET having a gate, a drain and a source; a second MOSFET (N13) comprising a second MOSFET having a gate, a drain and a source, the source of the first MOSFET being connected to the source of the second MOSFETthe drain of the first MOSFET being connected to the drain of the second MOSFET; so that the first MOSFET and the second MOSFET are in parallel and

together switch a load current equal to id; the first MOSFET being larger than the second MOSFET (column 3, lines 17-19). Thus, figure 2 shows all limitations of the claim except for the detail of the inverters 16-19. However, Wanlass' figure 5 shows an inverter comprising complementary MOS transistors (10, 30) connected between the supply terminals. Wanlass' inverter having the advantage of saving power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Wanlass's inverter for each of Lee inverters for the purpose of saving power consumption. Thus, the modified Lee's figure 2 further shows at least a third MOSFET (Wanlass' 10 in Lee's 19) comprising at least a third MOSFET die having a gate, a drain and a source for turning off the first MOSFET; the gate of the first MOSFET and the drain of the at least a third MOSFET being connected together; the source of the first MOSFET and the source of the at least a third MOSFET being connected together; at least a fourth MOSFET (Wanlass' 10 in Lee's 18) comprising at least a fourth MOSFET die having a gate, a drain and a source for turning off the second MOSFET; the gate of the second MOSFET and the drain of the at least a fourth MOSFET being connected together; the source of the second MOSFET and the source of the at least a fourth MOSFET being connected together; the gate of the first MOSFET being characterized by having a very low gate resistance (when Wanlass' transistor 10 is on, it's resistance is low. Therefore, the resistance at the gate of the first MOSFET is low); the on resistance of the at least a third MOSFET being characterized by having a very low channel resistance (when on); the gate of the second MOSFET being characterized by having a very low gate resistance; the on resistance of the at least a fourth MOSFET being characterized by having a very low channel resistance (when on); so that the third MOSFET may first be turned on so as to turn off the first MOSFET while the second

MOSFET remains conducting to limit the rise of the voltage on the common drain connection of the first MOSFET and the second MOSFET so that the gate voltage of the first MOSFET is reduced to a low voltage with no significant Miller current; and the fourth MOSFET may later be turned on so as to turn off the second MOSFET and interrupt the load current.

Allowable Subject Matter

10. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9-11 would be allowable because the prior art fails to teach that the source voltage is the drain of the first MOSFET.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

November 23, 2004